architecture requirements such that each memory slice has a number of registers provided by said system architecture and is arranged to supply respective bits of data, via a system bus of said register width requirement;

determining the depth of each of said memory slices based on the respective number of registers provided by said system architecture; and

establishing a default location that is initialized to zero ("0") in all subsequent memory slices which serves as a padding value when a memory location of a respective memory slice exceeding a register width of said memory slice is accessed, via said system bus.

22. The method as claimed in claim 21, wherein said memory is arranged to store context information needed for one or more Micro-Engines (MEs) in a host-fabric adapter to process host data transfer requests for data transfers.

23. The method as claimed in claim **22**, wherein, when a register width requirement is 32 bits, and a system architecture requires 15 registers of 8 bits, 8 registers of 12 bits, and 17 registers of 32 bits for a total of 40 registers, said memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into three memory slices, including